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SHALDON & MAK
225 SOUTH LAKE AVENUE
9TH FLOOR
PASADENA, CA 91101

EXAMINER	
CHU, CHRIS C	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 07/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/656,452	ELLSBERRY ET AL.	
	Examiner	Art Unit	
	Chris C. Chu	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 May 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 6, 8, 9, 11, 12, 15, 20, 21, 23, 24, 28 - 30 and 33 - 40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 6, 8, 9, 11, 12, 15, 20, 21, 23, 24, 28 - 30 and 33 - 40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Applicant's amendment filed on May 16, 2005 has been received and entered in the case.

Claim Objections

2. Claims 33 and 40 are objected to because of the following informalities:

   a. In claim 33, line 1, "first surfaces" should be --first surface--.

   b. In claim 40, line 2, "the memory semiconductor device" should be --memory die-- for consistence in the claims.

   Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 29 and 35 – 38 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

   c. In claim 29, line 2, "the memory device" lacks antecedent basis.

   d. In claim 35, line 5, "the memory die" lacks antecedent basis.

   e. In claim 37, lines 6 and 7, "the memory die" lacks antecedent basis.

f. Dependent claims 36 and 38 do not rectify the deficiency of claims 35 and 37 and therefore are similarly rejected.

g. For the examining purpose, Examiner treats the memory device or die in claims 29, 35 and 37 being the same device as the semiconductor device.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 15, 20, 28 and 35 are rejected under 35 U.S.C. 102(e) as being anticipated by Hayasaka et al. (6,809,421).

Regarding claim 15, Hayasaka et al. discloses in e.g., Fig. 33 a stackable electronic assembly comprising:

- a plurality of chip-scale packages (the packages in the Fig. 33), the plurality of chip-scale packages arranged in a stacked configuration (see Fig. 33), each chip-scale package including

- a substrate (152_2; column 25, lines 37 and 38) having a first surface and an opposite second surface, the substrate composed of a controlled thermal expansion material;
- a semiconductor device (151_2; column 25, line 37 and column 19, lines 42 – 47) coupled to traces on the first surface of the substrate using underside coupling members (160; column 25, line 58);
- a plurality of solder balls (157; column 25, line 48) mounted on the first surface of the substrate (152_2), at least one of the solder balls electrically coupled to the semiconductor device (see Fig. 33 and column 25, lines 55 – 57); and
- a plurality of pads (162; column 26, line 1) coupled to the second surface of the substrate, each pad electrically coupled to one or more of the plurality of solder balls (see Fig. 33),
- the substrate having a coefficient of expansion that matches a coefficient of expansion of the semiconductor device to within six parts per million per degree Celsius or less (column 26, lines 11 – 14).

Regarding claim 20, Hayasaka et al. discloses in e.g., Fig. 33 a memory module comprising:

- a main substrate (165; column 25, line 67) with an interface to couple the memory module to other devices; and
- one or more stacks of memory devices (the device in Fig. 33) coupled to a first surface of the main substrate (see Fig. 33),
  - at least one stack of memory devices (column 19, lines 41 – 49) including

- a plurality of chip-scale packages (the packages in Fig. 33), the plurality of chip-scale packages arranged in a stack, each chip-scale package including
  - a substrate (152_2; column 25, lines 37 and 38) having a first surface and an opposite second surface,
  - a memory semiconductor die (151_2; column 25, line 37 and column 19, lines 42 – 47) electrically coupled to traces on the first surface of the substrate (see Fig. 33 and column 25, lines 55 – 57),

- wherein the substrate (152_2) is composed of a controlled thermal expansion material, the substrate has a coefficient of expansion that matches a coefficient of expansion of the memory semiconductor die to within six parts per million per degree Celsius or less (column 26, lines 11 – 14).

Regarding claim 28, Hayasaka et al. discloses in e.g., Fig. 33 the semiconductor device (151_2) having a first surface and an opposite second surface, the first surface of the semiconductor device (151_2) mounted towards the first surface of the substrate (152_2), wherein the second surface of the semiconductor device (151_2) remains completely exposed for improved ventilation.

Regarding claim 35, Hayasaka et al. discloses in e.g., Fig. 33 a chip-scale package comprising:

- a substrate (152_2; column 25, lines 37 and 38) having a first surface and an opposite second surface, the substrate composed of a controlled thermal expansion material; and

- a semiconductor device (151_2; column 25, line 37 and column 19, lines 42 – 47) having a first surface and an opposite second surface, the first surface of the memory device (151_2) mounted facing the first surface of the substrate (152_2), the memory device (151_2) is electrically coupled to the substrate (see Fig. 33 and column 25, lines 55 – 57), the substrate having a coefficient of expansion that matches a coefficient of expansion of the memory device to within six parts per million per degree Celsius or less (column 26, lines 11 – 14), wherein the second surface of the memory device remains completely exposed (see e.g., Fig. 33).

7. Claims 35 – 38 are rejected under 35 U.S.C. 102(b) as being anticipated by Bertin et al. (U. S. Pat. No. 5,977,640).

Regarding claim 35, Bertin et al. discloses in e.g., Fig. 2 a chip-scale package comprising:

- a substrate (30; column 2, line 64) having a first surface and an opposite second surface, the substrate composed of a controlled thermal expansion material; and
- a semiconductor device (40; column 2, line 64) having a first surface and an opposite second surface, the first surface of the memory device (DRAM chip 40; column 4, lines 25 and 26) mounted facing the first surface of the substrate (30), the memory device (40) is electrically coupled to the substrate (column 2, lines 65 – 67), the substrate having a coefficient of expansion that matches a coefficient of expansion of the memory device to within six parts per million per degree Celsius or less (Since the substrate 30 and the semiconductor device 40 are chips, the material of the substrate 30 and the semiconductor device 40 are same. Thus, Bertin et al. fully

anticipates this limitation), wherein the second surface of the memory device remains completely exposed (see e.g., Fig. 2).

Regarding claim 36, Bertin et al. discloses in e.g., Fig. 2 the first surface of the memory device (40) remaining partially exposed for improved heat dissipation, the remaining five surfaces of the memory semiconductor device completely exposed for heat dissipation (see e.g., Fig. 2).

Regarding claim 37, Bertin et al. discloses in e.g., Fig. 6 a chip-scale package comprising:

- a substrate (30) having a first surface and an opposite second surface;
- a semiconductor device (40) mounted on the first surface of the substrate using a plurality of electrical conductors, the semiconductor device having a first surface and an opposite second surface, the first surface of the semiconductor device mounted facing the first surface of the substrate, wherein the first surface of the memory device remains partially exposed for improved heat dissipation (see e.g., Fig. 6); and
- a plurality of solder balls (the solder balls on the elements 32) mounted on the first surface of the substrate in a ball grid array configuration adjacent to the semiconductor device (see e.g., Fig. 6), at least one of the solder balls electrically coupled to the semiconductor device (column 4, lines 1 – 37).

Regarding claim 38, Bertin et al. discloses in e.g., Fig. 6 the second surface and remaining four surfaces of the memory semiconductor device being completely exposed for heat dissipation.

8. Claims 39 and 40 are rejected under 35 U.S.C. 102(e) as being anticipated by Kasatani (U. S. Pat. No. 6,617,695).

Regarding claim 39, Kasatani discloses in e.g., Fig. 7 and Fig. 8 a memory module (column 1, line 15) comprising:

- a main substrate (20; column 10, line 6) with an interface to couple the memory module to other devices (column 9, lines 45 – 47); and
- a plurality of chip-scale packages (34; column 9, line 37; see Fig. 7) arranged in one or more stacks, each stack coupled to the main substrate (20; see e.g., Figs. 7 and 8), each chip-scale package (34) including
  - o a substrate (11; column 9, line 37) having a first surface and an opposite second surface,
  - o a memory die (17; column 9, line 13) having a first surface and an opposite second surface, the first surface of the memory die mounted facing the first surface of the substrate (see e.g., Fig. 8),
  - o wherein the first surface of the memory die remains partially exposed for improved heat dissipation (see e.g., Figs. 6 and 8), and
  - o a plurality of solder balls (16; column 9, line 38) mounted on the first surface of the substrate in a ball grid array configuration adjacent to the memory die, at least one of the solder balls electrically coupled to the semiconductor device (column 9, lines 12 – 17 and lines 37 – 40).

Regarding claim 40, Kasatani discloses in e.g., Fig. 6 and Fig. 8 the second surface and remaining four surfaces of the memory semiconductor device (17) being completely exposed for heat dissipation.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 1 – 3, 5, 6, 8, 9, 11, 12, 23 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hayasaka et al. (6,809,421) in view of Nishimura et al. (U. S. Pat. No. 6,781,241).

Regarding claims 1, 23 and 30, Hayasaka et al. discloses in e.g., Fig. 33 a chip-scale package comprising:

- a substrate (152_2; column 25, lines 37 and 38) having a first surface and an opposite second surface, the substrate composed of a controlled thermal expansion material;
- a memory die (151_2; column 25, line 37 and column 19, lines 42 – 47) having a first surface and an opposite second surface, the first surface of the memory die (151_2) mounted facing the first surface of the substrate, the memory die (151_2) is electrically coupled to the substrate using a plurality of rigid underside coupling members (160; column 25, line 58), the substrate having a coefficient of expansion that matches a coefficient of expansion of the memory die to within six parts per million per degree

Celsius or less (column 26, lines 11 – 14), wherein the second surface of the memory die remains completely exposed (see e.g., Fig. 33);

- a plurality of solder balls (157; column 25, line 48) mounted on the first surface of the substrate in a ball grid array configuration adjacent to the memory die, at least one of the solder balls (157) electrically coupled to at least one of the underside coupling members (see Fig. 33 and column 25, lines 55 – 57);
- a plurality of pads (162; column 26, line 1) coupled to the second surface of the substrate (152_2), each pad electrically coupled to one or more of the plurality of solder balls (157; see Fig. 33).

Hayasaka et al. does not disclose one or more electronic components mounted on the second surface of the substrate in an area opposite of the die (claims 1 and 30) which is a dual inline module (claim 23), wherein the combined distance that an electronic component and the die protrude from the substrate is less than the distance that a solder ball and pad protrude from the substrate (claims 1 and 30). Nishimura et al. teaches in e.g., Fig. 10 one or more electronic components (3a under the element 1c; column 5, lines 13 and 14) mounted on the second surface of a substrate (1c; column 11, line 61) in an area opposite of a die (3b on the element 1c; column 11, line 60), wherein the combined distance that an electronic component and the die protrude from the substrate is less than the distance that a solder ball and pad protrude from the substrate (see Fig. 3 and column 5, line 66 – column 6, line 1). It would have been obvious to one of ordinary skill in the art at the time when the invention was made to apply the one or more electronic components to be mounted on the second surface of the substrate of Hayasaka et al. in

an area opposite of the memory die of Hayasaka et al. as taught by Nishimura et al. to improve a packaging density (column 2, lines 54 – 57).

Regarding claim 2, Hayasaka et al. discloses in e.g., Fig. 33 electrically conductive traces (column 25, lines 55 – 57) on the first surface to electrically couple at least one solder ball to the memory die directly (see Fig. 33 and column 25, lines 55 – 57).

Regarding claim 3, Hayasaka et al. discloses in e.g., Fig. 33 the plurality of rigid underside coupling members (160) being a second plurality of solder balls (column 25, line 58).

Regarding claims 5, 6 and 8, Hayasaka et al. discloses in e.g., Fig. 33 a chip-scale package comprising:

- a substrate (152_2; column 25, lines 37 and 38) having a first surface and an opposite second surface;
- a semiconductor device (151_2; column 25, line 37 and column 19, lines 42 – 47) mounted on the first surface of the substrate using a plurality of electrical conductors (160; column 25, line 58),
    - o the semiconductor device (151_2) having a first surface and an opposite second surface,
    - o the first surface of the semiconductor device (151_2) mounted facing the first surface of the substrate (152_2),
    - o wherein the second surface of the memory device (151_1) remains completely exposed for improved ventilation (see Fig. 33);
- a plurality of solder balls (157; column 25, line 48) mounted on the first surface of the substrate in a ball grid array configuration adjacent to the semiconductor device, at

least one of the solder balls electrically coupled to the semiconductor device (see Fig. 33 and column 25, lines 55 – 57); and

- a plurality of pads (162; column 26, line 1) coupled to the second surface of the substrate, each pad electrically coupled to one or more of the plurality of solder balls (157; see Fig. 33);
- which, when a plurality of chip-scale packages are stacked together (the packages in the Fig. 33), causes a solder ball (157) of a first chip-scale package to be uniquely electrically coupled with an electrical conductor of a semiconductor device mounted on a second chip-scale package N levels from the first chip-scale package.

Hayasaka et al. does not disclose the N level of the second chip-scale package being greater than two (claim 5); one or more electrical components being mounted on the second surface of the substrate (claim 6); and the combined distance that an electrical component and the semiconductor device protrude from the substrate being less than the distance that a solder ball and pad protrude from the substrate (claim 8). Nishimura et al. teaches in e.g., Fig. 10 the level of a second chip-scale package (the package that includes the element 1b) being greater than two (see Fig. 10); one or more electrical components (3a under the element 1c; column 5, lines 13 and 14) being mounted on the second surface of a substrate (1c; column 11, line 61) in an area substantially opposite of a semiconductor device (3b on the element 1c; column 11, line 60); and the combined distance that an electronic component and the die protrude from the substrate being less than the distance that a solder ball and pad protrude from the substrate (see Fig. 3 and column 5, line 66 – column 6, line 1). It would have been obvious to one of ordinary skill in the art at the time when the invention was made to apply the level of the second chip-

scale package of Hayasaka et al. being greater than two and the one or more electronic components to be mounted on the second surface of the substrate of Hayasaka et al. in an area opposite of the memory die of Hayasaka et al. as taught by Nishimura et al. to improve a packaging density (column 2, lines 54 – 57).

Regarding claim 9, Hayasaka et al. discloses in e.g., Fig. 33 the substrate (152_2) including a controlled thermal expansion material with a coefficient of expansion that "substantially" matches the coefficient of expansion of the semiconductor device (column 26, lines 11 – 14).

Regarding claim 11, Hayasaka et al. discloses in e.g., Fig. 33 electrically conductive traces on the first surface to electrically couple at least one solder ball to the semiconductor device (see Fig. 33 and column 25, lines 55 – 57).

Regarding claim 12, Hayasaka et al. discloses in e.g., Fig. 33 the semiconductor device being a silicon memory device (151_2; column 25, line 37 and column 19, lines 42 – 47).

11. Claims 4, 33 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hayasaka et al. and Nishimura et al. as applied to claims 1 and 5 above, and further in view of Kelly et al. (U. S. Pat. No. 5,798,567).

Regarding claims 4 and 33, while Hayasaka et al. and Nishimura et al. disclose five sides of the memory die (151_2) being completely exposed, Hayasaka et al. and Nishimura et al. do not disclose first surface of the semiconductor device being partially exposed. Kelly et al. teaches in e.g., Fig. 4 first surfaces (the surface where the solder ball 45 is located) of the semiconductor device being partially exposed. It would have been obvious to one of ordinary skill in the art at the time when the invention was made to apply the partially exposed first surface of the

semiconductor device of Hayasaka et al. and Nishimura et al. as taught by Nishimura et al. to decrease the manufacturing times and steps to produce the semiconductor package at low cost. Furthermore, the limitation "for the heat dissipation" is functional limitation that would not distinguish the claimed structure over Hayasaka et al., Nishimura et al. and Kelly et al.

Regarding claim 34, Hayasaka et al. and Nishimura et al. disclose the remaining four surfaces of the memory semiconductor device being completely exposed for heat dissipation.

12. Claims 21, 29 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hayasaka et al. in view of Kelly et al. (U. S. Pat. No. 5,798,567).

Regarding claims 21, 29 and 36, while Hayasaka et al. discloses five sides of the memory die (151_2) being completely exposed, Hayasaka et al. does not disclose first surface of the semiconductor device being partially exposed. Kelly et al. teaches in e.g., Fig. 4 first surfaces (the surface where the solder ball 45 is located) of the semiconductor device being partially exposed. It would have been obvious to one of ordinary skill in the art at the time when the invention was made to apply the partially exposed first surface of the semiconductor device of Hayasaka et al. as taught by Nishimura et al. to decrease the manufacturing times and steps to produce the semiconductor package at low cost. Furthermore, the limitation "for the heat dissipation" is functional limitation that would not distinguish the claimed structure over Hayasaka et al. and Kelly et al.

13. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hayasaka et al. (6,809,421) in view of Corisis et al. (6,414,391).

While Hayasaka et al. discloses the use of the memory module, Hayasaka et al. does not disclose another stack of memory devices on a second surface of the main substrate. Corisis et al. teaches in e.g., Fig. 4 another stack of memory devices (100, at the bottom) coupled to a second surface of a main substrate (50). It would have been obvious to one of ordinary skill in the art at the time when the invention was made to apply the another stack of memory devices on a second surface of the main substrate of Hayasaka et al. as taught by Nishimura et al. to form highly dense components (column 4, lines 35 – 37).

Response to Arguments

14. Applicant's arguments with respect to claims 1, 5, 15 and 20 have been considered but are moot in view of the new grounds of rejection.

Conclusion

15. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chris C. Chu whose telephone number is 571-272-1724. The examiner can normally be reached on 11:30 - 8:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 517-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov.

Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chris C. Chu
Examiner
Art Unit 2815

c.c.
Monday, July 18, 2005

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER